REMARKS

Entry of the above amendments is respectfully requested. Claims 1, 13, 14, 16, 17, 18, 23, 28, 29, 32, 39, 48, 51, and 52 have been amended. Claims 15, 24, 33, 49, and 50 have been cancelled. Claims 53-102 have been added. Claims 1-14, 16-23, 25-32, 34-48, and 51-102 are pending in the application. Favorable reconsideration and allowance of this application is respectfully requested in light of the foregoing amendments and the remarks which follow.

I. Claim Rejections - 35 USC § 112

The Office Action rejects claims 1, 13, 17-18, and 51-52 under 35 USC § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention.

In particular, claim 1 is rejected because there is insufficient antecedent basis for the limitation "the recess" recited in line 8. Claim 1 has been amended to overcome this rejection. Applicant asserts that this amendment does not limit or in any way narrow the claim element, but rather enhances the clarity of claim 1.

Claim 13 is rejected because the limitation "thinning the substrate such that the alignment hole..." is indefinite. The claim has been amended to clarify that the wafer is thinned.

Claims 17-18 are rejected because the limitation "first and second layers" in line 2 of claim 17 lacks antecedent basis. Claim 17 is also rejected because the limitation "etching an alignment hole ... through the substrate" in line 2 is indefinite. Claim 17 has been amended to recite "first and second members" and also to recite "etching an alignment hole ... through the wafer" to overcome the rejections. Applicant notes that these amendments do not limit or in any way narrow the claim, but rather enhance the clarity of claim 17.

Claims 51-52 are rejected because the limitation "etching an alignment hole ... through the substrate" in line 2 is indefinite. Claim 51 has been amended to recite "etching an alignment hole ... through the wafer" to overcome the rejection. Applicant notes that these amendments do not limit or in any way narrow the claim, but rather enhance the clarity of claim 51.

All rejections made pursuant to 35 USC § 112 have been overcome. Accordingly, withdrawal of the rejection of claims 1-7 under 35 USC § 112 is respectfully requested.

II. Claim Rejections - 35 USC § 102

A. Claim 1

The Office Action rejects claims 1-2 under 35 USC § 102(e) as being anticipated by Greywall. Greywall teaches a method for fabricating an optical cavity having two mirrors, at least one of which is movable. These structures are achieved by patterning and attaching two SOI wafers. (See Abstract).

Amended claim 1 presents several limitations that are neither taught nor suggested by Greywall or any other cited reference, when properly viewed either alone or in combination.

For instance, the Office Action cites Fig. 7I, col. 10, lines 45-50 to assert that Greywall discloses a step of, after step (b), attaching the wafer to the upper surface of a substrate to form a composite structure having an internal void formed therein. Greywall, however, does not disclose this limitation recited in claim 1. Rather, Greywall discloses providing two SOI wafers 200C and 200D that are prepatterned and attached to each another to form a structure having regions 720 and 710, respectively, that will provide the mirrors. (Col. 10, lines 13-45) Accordingly, Greywall does not disclose attaching the wafer to an upper surface of a substrate as originally recited in claim 1.

Claim 1 has been further amended to clarify that the substrate provides at least one wall that at least partially defines the void. Greywall does not disclose such an arrangement, as the void (Gap "G" in Fig. 7I) is defined by wafers 200C and 200D along with standoff 716. Greywall in fact teaches away from implementing the claimed method fabrication recited in claim 1. In particular, Greywall's SOI wafers must be attached to each other in order to provide the optical cavity having opposing mirrors located at opposite sides of the void. If one of the Greywall's wafers was attached to a substrate having a wall that partially define the void, Greywall would be incapable of forming the opposing sets of mirrors.

Applicant does not assert that selectively etching a layer of material in a multi-layer wafer is independently novel, nor does Applicant assert that bonding a wafer to a substrate is independently novel. However, the step of selectively etching a layer of material in a multi-layer wafer to form a bridge, and subsequently attaching that wafer to a substrate to form an internal void that is at least partially defined by the substrate is neither taught nor suggested in the prior art. The claimed method furthermore provides advantages not realized by prior art techniques.

For example, the Kawai reference, which is cited against other pending claims in the present application, discloses that a silicon wafer 2 is partially etched to form a groove 15 prior to attaching the wafer to a substrate. (Fig. 5) This etching technique requires that the etchant is precisely controlled both in terms of amount used and duration of etching in order to provide a groove, and subsequently a vibrator 14, of a desired size and configuration. Even if applied in the desired manner, the etchant may nevertheless act in an unpredictable manner to produce undesirable results. The present invention, on the contrary, recognizes that one may take advantage of a multi-layer wafer to control the size and shape of the recess by selectively etching one of the layers prior to attaching the wafer to a substrate.

Accordingly, Greywall does not disclose all elements of amended claim 1 and furthermore teaches away from the claim elements. Moreover, because amended claim 1 is further nonobvious over Greywall in view of Kawai, Applicant asserts that claim 1 is patentable over the cited references. Withdrawal of the rejection of claim 1 under §102 is therefore respectfully requested.

B. Claims 16, 19, 25, and 28

Independent claim 16 recites removing a portion of the first member of a wafer to form a bridge and a pair of spacers defining a recess therebetween. The spacers are then attached to a substrate to form a composite structure having an internal void formed therein. As discussed above with respect to claim 1, Greywall does not disclose the step of attaching spacers of a wafer to a substrate to form a composite structure having an internal void. Rather, Greywall attaches standoff 716 to another wafer 200C, not a substrate, to form a composite structure. Also as discussed above, Greywall teaches away from attaching standoff 716 to a substrate as doing so would prevent the formation of the second set of mirrors 710. Additionally, because Kawai does attach a wafer directly to a substrate, Applicant asserts that no teaching or suggestion exists to combine these references to produce the presently claimed invention. Claim 16 has been further amended to recite the substrate having a wall that at least partially defines the void to further distinguish the present invention from Greywall.

Applicant therefore asserts that independent claim 16 along with corresponding dependent claims 19, 25, and 28 are patentable over the cited references. Withdrawal of the rejection of claims 16, 19, 25, and 28 under §102 is respectfully requested.

III. Claim Rejections – 35 USC §103

A. Paragraph 4 of Office Action

The Office Action rejects claims 7-9, 29, 35, 39, and 45 under 35 USC § 103(a) as being unpatentable over Greywall in view of Kawai.

Claims 7-9

Applicant asserts the allowability of independent claim 1 as a sufficient basis for the allowance of corresponding dependent claims 7-9. Withdrawal of the rejection of claims 7-9 under §103 is respectfully requested.

Claim 29

Independent claim 29 recites a method of fabricating a MEMS structure. In particular, a wafer is provided and a pair of spacers are formed at opposite ends of a surface of a wafer. A recess is defined between the spacers. Next, a layer is deposited onto the upper surface of the wafer in the recess and a portion of the layer is etched to define a bridge, as illustrated in Figs. 8-9. The spacers are then attached to a substrate, and the wafer is etched to release the bridge.

None of the cited references teach or suggest depositing a layer onto the upper surface of the wafer in the recess and etching a portion of the layer to define a bridge. As discussed above, Greywall discloses etching a pre-existing layer of a wafer to form a bridge, and subsequently attaching that wafer to a second wafer to form a composite structure. Kawai merely discloses partially etching into a single-layer wafer to form a recess. While Kawai does disclose the presence of an independent layer within an internal void (See Fig. 5), layer 18 is an electrode plate, and does not provide the claimed bridge in subsequent etching steps. Rather, wafer 24 is etched to provide a bridge 14 as illustrated in Fig. 6. However, bridge 14 is not formed by depositing and patterning a layer onto the wafer. Accordingly, even when the references are combined in the manner suggested in the Office Action, the combination fails to teach or suggest all recited elements in claim 29.

The invention as recited in claim 29 furthermore provides the advantage of enabling one to produce a multi-layer movable MEMS element from a single-layer wafer. and produce a selectively etchable layer of material on the wafer. (See Figs. 8-11) Accordingly, a bridge may be produced and subsequently released that includes the

deposited layer (such as an insulator) and a conductive layer (such as silicon from the wafer) extending outwardly from the bridge.

This advantage is not recognized in the prior art. In fact, Kawai teaches away from this claim by etching a single-layer wafer to form a recess, and etching into that wafer to release an inner portion (See Figs. 4-6). Kawai therefore does not recognize the advantages of depositing a layer of material onto the wafer that would ultimately provide a bridge.

Accordingly, withdrawal of the rejection of claim 29 under §103 is respectfully requested.

Claim 35

Independent claim 35, similar to claim 29, recites the steps of partially etching into a surface of the wafer to form a recess therein disposed between a pair of spacers, and depositing a layer onto the surface of the wafer in the recess so as to form a bridge. The spacers are attached to a substrate to define an internal void, and the wafer is etched to release the bridge. As discussed above, none of the cited references teach or suggest, either alone or in combination, the step of depositing a layer onto the surface of the wafer in the recess to form a bridge. Accordingly, withdrawal of the rejection of claim 35 under §103 is respectfully requested.

Claims 39 and 45

Independent claim 39 recites etching one layer of a multi-layer wafer to produce a bridge, and etching a recess into a substrate before attaching the wafer to the substrate. Next, the wafer is etched to release the bridge from mechanical communication with the substrate. As discussed above, none of the cited references teach or suggest producing a bridge from a multi-layer wafer and attaching the wafer to a substrate to define a composite structure having an internal void, and subsequently etching the wafer to release the bridge. Claim 39 further recites the step of etching a recess into a surface of the substrate to produce the void when the wafer is attached to the substrate.

The Office Action cites Kawai (at Fig. 7 Col, 9, lines 13-22) to assert that the reference teaches or suggests the claim limitations. However, the Kawai discloses that substrate 3 is an *upper* substrate having a closed space 4 that covers the detecting element 11. The substrate recited in claim 39 is easily distinguished from the cited substrate in Kawai.

For instance, claim 39 recites that the wafer is attached to the surface of the substrate to form an internal void such that the bridge is disposed between the surface the substrate and the second layer of the wafer. In Kawai, the upper substrate 3 is not attached to wafer 2 until the bridge 14 is already formed. Furthermore, Kawai fails to disclose a second layer of the wafer. Granted, Greywall discloses a wafer having a first and second layer. However, even if the two references are combined in the manner suggested by the Office Action, no teaching or suggestion exists to position the bridge between the surface of the substrate and the second layer of the wafer. In Greywall, the bridge is disposed between two wafers. In Kawai, the bridge 14 is disposed between two substrates. No teaching suggests to modify either of the references to produce a bridge disposed between a wafer and a substrate.

Additionally, claim 39 recites etching through the second layer to release the bridge from mechanical communication with the substrate. As stated above, substrate 3 is not connected to wafer 2 until the bridge 14 is already formed and released (See Fig. 6). The void in Fig. 6 is formed by partially etching into the wafer 17, and not by forming a groove in the substrate 3. Accordingly, the bridge 14 is released from substrate 1 and not substrate 3. (See Col. 9, lines 1-12).

For at least these reasons, the cited references even when combined in the manner suggested in the Office Action fail to teach or suggest all claim limitations. Furthermore, as discussed above, the references teach away from combination with one another to produce the presently claimed invention. Accordingly, withdrawal of the rejections of claim 35 and corresponding dependent claim 45 under §103 is respectfully requested.

B. Paragraph 5 of Office Action

In Paragraph 5 of the Office Action, claims 4-6, 28, and 42-44 are rejected under §103 as being unpatentable over Greywall in view of Kawai, and further in view of Coldren. Applicant asserts the patentability of independent claims 1, 16, and 39 as a sufficient basis for the allowability of corresponding dependent claims 4-6, 28, and 42-44, respectively.

As to claims 4 and 42, the Office Action cites Coldren at column 3, lines 26-30 as disclosing the interchangeable use of substrates from various materials. In particular, Coldren discloses several materials that may comprise substrate 10 rather than the claimed wafer. Furthermore, Coldren's substrate 10 differs both structurally and

functionally from the claimed wafer that provides active material that is patterned to form the MEMS device. Coldren's substrate 10 merely provides a platform that supports various wafers that are patterned to provide a device. Substrate 10 is analogous to the substrate 14 of Fig. 1 in the pending application. Claims 4 and 42 recite materials of the claimed wafer and not the substrate. Accordingly, even when Coldren is combined with the other cited references, the combination fails to teach or suggest all claim limitations recited in claims 4 and 42.

For at least these reasons, withdrawal of the §103 rejection of claims 4-6, 28, and 42-44 is respectfully requested.

C. Paragraph 6 of Office Action

In paragraph 6 of the Office Action, claims 2-3, 26-27, 34, 38, and 40-41 are rejected under 35 U.S.C. §103 as being unpatentable over Greywall in view of Kawai, and further in view of Jacobsen. Applicant submits that the patentability of independent claims 1, 16, 29, 35, and 39 provides a sufficient basis for the allowability of these dependent claims.

Furthermore, Applicant submits that the combination of Jacobsen with Greywall and Kawai is improper. Greywall and Kawai both disclose methods of fabricating a MEMS device, while Jacobsen relates to the fabrication of a display panel. Moreover, while Jacobsen discloses a conductive layer, Applicant does not assert that the mere presence of a conductive layer deposited onto a preexisting layer is patentable. However claims 2, 26, 34, 38, and 40 recite the step of depositing a conductive layer onto a wafer of a MEMS device that is fabricated without undercutting a sacrificial layer. The conductive layer forms the electrical contact for the MEMS structure (See Paragraph 76). Applicant has found no disclosure in Jacobsen that would motivate one having ordinary skill in the art to apply a conductive layer onto a wafer of a MEMS structure.

For at least these additional reasons, Applicant asserts that dependent claims 2, 26, 34, 38, and 40, along with corresponding dependent claims 3, 27, and 41, are allowable over the cited references. Withdrawal of the §103 rejection of claims 2-3, 26-27, 34, 38, and 40-41 is therefore respectfully requested.

D. Paragraph 7 of Office Action

In paragraph 7 of the Office Action, claims 10-11, 20-22, 30-31, 36-37, and 46-47 are rejected under 35 U.S.C. §103 as being unpatentable over Greywall in view of Kawai,

and further in view of Huibers. Applicant submits that the patentability of claims 1, 16 and 19, 29, 35, and 39 provides a sufficient basis for the allowability of these dependent claims. Accordingly, withdrawal of the §103 rejection of these claims is respectfully requested.

E. Paragraph 8 of Office Action

In paragraph 8 of the Office Action, claims 12-13, 17-18, and 51-52 are rejected under 35 U.S.C. §103 as being unpatentable over Greywall in view of Kawai, and further in view of McNie. Applicant submits that the patentability of claims 1, 16, and 39 provides a sufficient basis for the allowability of these dependent claims. Accordingly, withdrawal of the §103 rejection of these claims is respectfully requested.

IV. Allowable Subject Matter

Applicant notes with appreciation the indication in Paragraph 9 of the Office Action that claims 14-15, 23-24, 32-33, and 38-50 contain allowable subject matter. Claims 14, 23, 32, and 38 have been rewritten in independent form as new claims 53, 68, 81, and 90, respectively. New dependent claims 54-67, 69-80, 82-85, and 91-102 are intended generally to correspond to dependent claims originally filed with the application.

Furthermore, new independent claim 86 has been added that corresponds roughly to pending independent claim 35. However, step (e) of claim 86 includes the step of producing a stationary conductive MEMS element attached to the substrate, and a movable conductive MEMS element supported by the bridge and separated by the stationary element via a variable size gap. As stated in paragraph 9 of the Office Action, none of the references of record teach or suggest such a method. Dependent claims 87-89 are intended to correspond to claims 36-38 as originally filed.

Accordingly, formal allowance of new claims 53-102 is respectfully requested.

V. Conclusion

Applicant therefore respectfully asserts that all rejections and objections cited by the Examiner have been overcome. Accordingly, the application is in condition for allowance, and a Notice of Allowance is earnestly solicited. The Examiner is invited to contact the undersigned at the telephone number appearing below if such would advance the prosecution of this application.

The Commissioner is hereby authorized to deduct the $1230 fee for the addition of 5 independent claims in excess of three at $84 per claim, and the addition 45 claims in

excess of twenty at $18 per claim along with any other fees arising from this or any other communication, from Deposit Account No. 17-0055.

Respectfully submitted,

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VERSION OF CLAIMS WITH MARKINGS TO SHOW CHANGES MADE

1. (Once Amended) A method of fabricating a MEMS structure, comprising the steps of:

(f) providing a wafer having at least a first layer and a second layer;

(g) removing a portion of the first layer through to the second layer to form a bridge member;

(c) after step (b), attaching the wafer to the upper surface of [the] a substrate to form a composite structure having an internal void formed therein, wherein the bridge member is aligned with the internal void, and wherein the substrate provides at least one wall that at least partially defines the void; and

(d) etching through the [upper] second layer of the wafer around the periphery of the bridge member to break through into the [recess] void, thereby releasing the bridge from the substrate.

2. The method as recited in claim 1, further comprising depositing a conductive layer onto the wafer.

3. The method as recited in claim 2, wherein the conductive layer is selected from the group consisting of aluminum, copper, silver, gold and nickel.

4. The method as recited in claim 1, wherein the wafer is selected from the group consisting of silicon, silicon carbide and gallium arsenide.

5. The method as recited in claim 1, wherein the substrate is a non-conductive substrate selected from the group consisting of glass, high resistivity silicon, crystalline sapphire, and ceramic.

6. The method as recited in claim 1, wherein the substrate is a conductive substrate selected from the group consisting of silicon, silicon carbide, and gallium arsenide.

7. The method as recited in claim 1, wherein the void is formed by pre-patterning a recess into a surface of the wafer prior to step (c), and bonding the surface to the substrate.

8. The method as recited in claim 1, wherein the void is formed by pre-patterning a recess into a surface of the substrate prior to step (c), and bonding the surface to the wafer.

9. The method as recited in claim 1, wherein the recess has beveled edges.

10. The method as recited in claim 1, wherein the bridge member comprises an insulating material.

11. The method as recited in claim 10, wherein the bridge member comprises silicon dioxide.

12. The method as recited in claim 1, further comprising etching an alignment hole into the wafer.

13. (Once Amended) The method as recited in claim 12, further comprising thinning the [substrate] wafer such that the alignment hole extends entirely through the [substrate] wafer.

14. (Once Amended) The method as recited in claim 1, wherein step (d) further comprises forming a stationary conductive member extending from the substrate that is separated from the bridge [via a forming a conductive member extending from the bridge and separated from a stationary member] via a variable size gap.

15. Cancelled

16. (Once Amended) A method of fabricating a MEMS structure, comprising the steps of:

(a) providing a wafer having at least a first member and a second member;

(b) removing a portion of the first member through to the second member to form a bridge and a pair of spacers defining a recess therebetween;

(c) attaching the spacers to a substrate to form a composite structure having an internal void formed therein, wherein the bridge is aligned with the internal void, and wherein the substrate provides at least one wall that at least partially defines the internal void; and

(d) etching through the second member around the periphery of the bridge to break through into the recess and release the second member from mechanical communication with the substrate.

17. The method as recited in claim 16, further comprising etching an alignment hole through the first, and second [layers] members and substantially through the [substrate] wafer.

18. The method as recited in claim 17, further comprising thinning the [substrate] wafer such that the alignment hole extends entirely through the [substrate] wafer.

19. The method as recited in claim 16, wherein the first member comprises a first layer and a second layer of selectively etchable materials, wherein the first layer is etched to form the spacers, and wherein the second layer is etched to form the bridge.

20. The method as recited in claim 19, wherein the second layer is made of an insulating material.

21. The method as recited in claim 20, wherein the second layer comprises silicon dioxide.

22. The method as recited in claim 19, wherein the first layer is selected from the group consisting of silicon nitride and polycrystalline silicon.

23. (Once Amended) The method as recited in claim 16, wherein step (d) further comprises forming a stationary conductive member extending from the substrate that is separated from the bridge [conductive member extending from the bridge and separated from a stationary member] via a variable size gap

24. Cancelled

25. The method as recited in claim 16, wherein the second member comprises silicon.

26. The method as recited in claim 16, further comprising depositing and patterning a conductive layer onto the first layer.

27. The method as recited in claim 26, wherein the conductive layer comprises aluminum.

28. (Once Amended) The method as recited in claim 16, wherein the substrate is selected from the group consisting of glass, high resistivity silicon, crystalline sapphire, crystalline silicon, polycrystalline silicon, silicon carbide, or ceramic.

29. (Once Amended) A method of fabricating a MEMS structure, comprising the steps of:

(a) providing a wafer;

(b) forming a pair of spacers at opposite ends of a surface of the wafer, wherein the spacers define a recess therebetween;

(h) depositing a layer onto the [upper surface of the] wafer in the recess;

(i) etching a portion of the layer to define a bridge;

(j) attaching the spacers to a substrate to define an internal void; and

(k) etching through the wafer into the void around the periphery of the bridge to release the bridge from mechanical communication with the substrate.

30. The method as recited in claim 29, wherein the layer is insulating.

31. The method as recited in claim 30, wherein the layer comprises silicon dioxide.

32. (Once Amended) The method as recited in claim 29, wherein step (f) further comprises producing a stationary conductive MEMS element separated from the bridge via a variable size gap. [attached to the substrate, and a movable conductive MEMS element supported by the bridge.]

33. Cancelled

34. The method as recited in claim 29, further comprising depositing a conductive layer onto the wafer.

35. A method of fabricating a MEMS structure, comprising the steps of:

(a) providing a wafer;

(b) partially etching into a surface of the wafer to form a recess therein disposed between a pair of spacers;

(c) depositing a layer onto the surface of the wafer in the recess so as to form a bridge;

(d) attaching the spacers to a substrate to define an internal void; and

(e) etching through the wafer into the void around the periphery of the bridge to release the bridge from mechanical communication with the substrate.

36. The method as recited in claim 35, wherein the layer is insulating.

37. The method as recited in claim 36, wherein the layer comprises silicon dioxide.

38. The method as recited in claim 35, further comprising depositing a conductive layer onto the wafer.

39. (Once Amended) A method of fabricating a MEMS structure, comprising the steps of:

(a) providing a wafer having at least a first and a second layer;

(b) etching into the first layer to produce a bridge;

(c) providing a substrate;

([c]d) etching a recess into a surface of the substrate;

([d]e) after step (b), attaching the wafer to the surface of the substrate to form an internal void such that the bridge is 1) disposed between the surface and the second layer, and 2) aligned with the void; and

([e]f) etching through the second layer around the periphery of the bridge to release the bridge from mechanical communication with the substrate.

40. The method as recited in claim 39, further comprising depositing a conductive layer onto the wafer.

41. The method as recited in claim 40, wherein the conductive layer is selected from the group consisting of aluminum, copper, silver, gold and nickel.

42. The method as recited in claim 39, wherein the wafer is selected from the group consisting of silicon, silicon carbide and gallium arsenide.

43. The method as recited in claim 39, wherein the substrate is a non-conductive substrate selected from the group consisting of glass, high resistivity silicon, crystalline sapphire, and ceramic.

44. The method as recited in claim 39, wherein the substrate is a conductive substrate selected from the group consisting of silicon, silicon carbide, and gallium arsenide.

45. The method as recited in claim 39, wherein the recess has beveled edges.

46. The method as recited in claim 39, wherein the bridge member comprises an insulating material.

47. The method as recited in claim 46, wherein the bridge member comprises silicon dioxide.

48. (Once Amended) The method as recited in claim 39, wherein step ([e]f) further comprises producing a stationary conductive MEMS element attached to the substrate separated from the bridge via a variable size gap.[, and a movable conductive MEMS element supported by the bridge.]

49. Cancelled

50. Cancelled

51. (Once Amended) The method as recited in claim 39, further comprising etching an alignment hole through the first and second layers, and partially through the [substrate] wafer.

52. (Once Amended) The method as recited in claim 51, further comprising thinning the [substrate] wafer such that the alignment hole extends entirely through the [substrate] wafer.

53. (New) A method of fabricating a MEMS structure, comprising the steps of:

(a) providing a wafer having at least a first layer and a second layer;

(b) removing a portion of the first layer to form a bridge member;

(c) after step (b), attaching the wafer to a substrate to form a composite structure having an internal void formed therein, wherein the bridge member is aligned with the internal void; and

(d) etching through the second layer of the wafer around the periphery of the bridge member to break through into the void, thereby releasing the bridge from the substrate and forming a conductive member extending from the bridge separated from a stationary member by a variable size gap.

54. The method as recited in claim 53, further comprising depositing a conductive layer onto the wafer.

55. (New) The method as recited in claim 54, wherein the conductive layer is selected from the group consisting of aluminum, copper, silver, gold and nickel.

56. (New) The method as recited in claim 53, wherein the wafer is selected from the group consisting of silicon, silicon carbide and gallium arsenide.

57. (New) The method as recited in claim 53, wherein the substrate is a non-conductive substrate selected from the group consisting of glass, high resistivity silicon, crystalline sapphire, and ceramic.

58. (New) The method as recited in claim 53, wherein the substrate is a conductive substrate selected from the group consisting of silicon, silicon carbide, and gallium arsenide.

59. (New) The method as recited in claim 53, wherein the void is formed by pre-patterning a recess into a surface of the wafer prior to step (c), and bonding the surface to the substrate.

60. (New) The method as recited in claim 53, wherein the void is formed by pre-patterning a recess into a surface of the substrate prior to step (c), and bonding the surface to the wafer.

61. (New) The method as recited in claim 53, wherein the recess has beveled edges.

62. (New) The method as recited in claim 53, wherein the bridge member comprises an insulating material.

63. (New) The method as recited in claim 62, wherein the bridge member comprises silicon dioxide.

64. (New) The method as recited in claim 53, further comprising etching an alignment hole into the wafer.

65. (New) The method as recited in claim 64, further comprising thinning the wafer such that the alignment hole extends entirely through the wafer.

66. (New) The method as recited in claim 53, wherein step (d) further comprises forming the stationary member extending outwardly from the substrate.

67. (New) The method as recited in claim 53, wherein the conductive member and stationary member are electrically isolated from one another.

68. (New) A method of fabricating a MEMS structure, comprising the steps of:

(a) providing a wafer having at least a first member and a second member;

(b) removing a portion of the first member to form a bridge and a pair of spacers defining a recess therebetween;

(c) attaching the spacers to a substrate to form a composite structure having an internal void formed therein, wherein the bridge is aligned with the internal void; and

(d) etching through the second member around the periphery of the bridge to break through into the recess and release the second member from mechanical communication with the substrate, wherein the etching step forms a conductive member extending from the bridge and separated from a stationary member via a variable size gap.

69. (New) The method as recited in claim 68, further comprising etching an alignment hole through the first, and second layers and substantially through the wafer.

70. (New) The method as recited in claim 69, further comprising thinning the wafer such that the alignment hole extends entirely through the wafer.

71. (New) The method as recited in claim 68, wherein the first member comprises a first layer and a second layer of selectively etchable materials, wherein the first layer is etched to form the spacers, and wherein the second layer is etched to form the bridge.

72. (New) The method as recited in claim 71, wherein the second layer is made of an insulating material.

73. (New) The method as recited in claim 72, wherein the second layer comprises silicon dioxide.

74. (New) The method as recited in claim 71, wherein the first layer is selected from the group consisting of silicon nitride and polycrystalline silicon.

75. (New) The method as recited in claim 68, wherein step (d) further comprises forming the stationary member extending outwardly from the substrate.

76. (New) The method as recited in claim 68, wherein the conductive member and stationary member are electrically isolated from one another.

77. (New) The method as recited in claim 68, wherein the second member comprises silicon.

78. (New) The method as recited in claim 68, further comprising depositing and patterning a conductive layer onto the first layer.

79. (New) The method as recited in claim 78, wherein the conductive layer comprises aluminum.

80. (New) The method as recited in claim 68, wherein the substrate is selected from the group consisting of glass, high resistivity silicon, crystalline sapphire, crystalline silicon, polycrystalline silicon, silicon carbide, or ceramic.

81. (New) A method of fabricating a MEMS structure, comprising the steps of:

(a) providing a wafer;

(b) forming a pair of spacers at opposite ends of a surface of the wafer, wherein the spacers define a recess therebetween;

(c) depositing a layer onto the wafer in the recess;

(d) etching a portion of the layer to define a bridge;

(e) attaching the spacers to a substrate to define an internal void; and

(f) etching through the wafer into the void around the periphery of the bridge to release the bridge from mechanical communication with the substrate and to produce a stationary conductive MEMS element attached to the substrate, and a movable conductive MEMS element supported by the bridge.

82. (New) The method as recited in claim 81, wherein the layer is insulating.

83. (New) The method as recited in claim 82, wherein the layer comprises silicon dioxide.

84. (New) The method as recited in claim 81, wherein the conductive member and stationary member are electrically isolated from one another.

85. (New) The method as recited in claim 81, further comprising depositing a conductive layer onto the wafer.

86. (New) A method of fabricating a MEMS structure, comprising the steps of:

(a) providing a wafer;

(b) partially etching into a surface of the wafer to form a recess therein disposed between a pair of spacers;

(d) depositing a layer onto the surface of the wafer in the recess so as to form a bridge;

(d) attaching the spacers to a substrate to define an internal void; and

(e) etching through the wafer into the void around the periphery of the bridge to release the bridge from mechanical communication with the substrate and to produce a stationary conductive MEMS element attached to the substrate, and a movable conductive MEMS element supported by the bridge and separated by the stationary element via a variable size gap.

87. (New) The method as recited in claim 86, wherein the layer is insulating.

88. (New) The method as recited in claim 87, wherein the layer comprises silicon dioxide.

89. (New) The method as recited in claim 86, further comprising depositing a conductive layer onto the wafer.

90. (New) A method of fabricating a MEMS structure, comprising the steps of:

(a) providing a wafer having at least a first and a second layer;

(b) etching into the first layer to produce a bridge;

(c) providing a substrate;

(d) etching a recess into a surface of the substrate;

(e) after step (b), attaching the wafer to the surface of the substrate to form an internal void such that the bridge is 1) disposed between the surface and the second layer, and 2) aligned with the void; and

(f) etching through the second layer around the periphery of the bridge to release the bridge from mechanical communication with the substrate and to produce a stationary conductive MEMS element attached to the substrate, and a movable conductive MEMS element supported by the bridge.

91. (New) The method as recited in claim 90, further comprising depositing a conductive layer onto the wafer.

92. (New) The method as recited in claim 91, wherein the conductive layer is selected from the group consisting of aluminum, copper, silver, gold and nickel.

93. (New) The method as recited in claim 90, wherein the wafer is selected from the group consisting of silicon, silicon carbide and gallium arsenide.

94. (New) The method as recited in claim 90, wherein the substrate is a non-conductive substrate selected from the group consisting of glass, high resistivity silicon, crystalline sapphire, and ceramic.

95. (New) The method as recited in claim 90, wherein the substrate is a conductive substrate selected from the group consisting of silicon, silicon carbide, and gallium arsenide.

96. (New) The method as recited in claim 90, wherein the recess has beveled edges.

97. (New) The method as recited in claim 90, wherein the bridge member comprises an insulating material.

98. (New) The method as recited in claim 97, wherein the bridge member comprises silicon dioxide.

99. (New) The method as recited in claim 90, wherein the conductive member and stationary member are electrically isolated from one another.

100. (New) The method as recited in claim 90, wherein step (f) further comprises forming a conductive member extending from the bridge and separated from the stationary member via a variable size gap.

101. (New) The method as recited in claim 90, further comprising etching an alignment hole through the first and second layers, and partially through the wafer.

102. (New) The method as recited in claim 101, further comprising thinning the substrate such that the alignment hole extends entirely through the wafer.